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10/562,237	03/29/2006	Wolfgang Kemper	DE03 0231 US1	3782

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EXAMINER	
THOMAS, LUCY M	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
01/15/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/562,237	KEMPER, WOLFGANG	
	Examiner	Art Unit	
	Lucy Thomas	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6, 8, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Krakauer et al. (US 5,617,283). Regarding Claim 1, Krakauer discloses an integrated protection circuit for an integrated circuit device (Figures 1-2), comprising: a first transistor 45a (Figure 2) whose control outputs are connected between a pad 12 and a control input of a clamping device 18, control outputs of said clamping device being connected between said pad and a reference voltage terminal VSS, a second transistor 45b whose control input of the clamping device and said reference voltage terminal, and time-delay means (circuit connection of 42 including the connection means) connected to a supply voltage terminal 16 and said control inputs of said first transistor and said second transistor.

Regarding Claim 2, Krakauer discloses that the pad is a signal pad or a power supply pad.

Regarding Claim 3, Krakauer discloses that the time- delay element comprises a series connection of a resistor and a capacitance (see series connection of resistor formed by the connection or well resistance, and the capacitor formed by the capacitance of the 42).

Regarding Claim 4, Krakauer discloses that the time delay means comprises a third transistor 42, the resistor being connected between the supply voltage terminal and said third transistor, said third transistor forming the capacitance.

Regarding Claims 6 and 8, Krakauer discloses that the first transistor (MP1) is a p-channel MOS transistor (45a is a PMOS transistor), and the clamping device is an n-channel MOS transistor laid out for ESD protection (see Figure 2).

Regarding Claim 9, Krakauer discloses a clamping device which forms a parasitic npn transistor.

Regarding Claim 12, Krakauer discloses an integrated protection circuit for protecting an integrated circuit device, the protection circuit comprising: a clamping device 18 having a control input and two control outputs, the control outputs including a first control output coupled to a pad 12 and a second control output coupled to a reference voltage terminal V_{SS}; a first transistor 45a having control outputs connected between the pad and the control input of the clamping device; a second transistor 45b having control outputs connected between the reference voltage terminal and the control input of the clamping device; and a time-delay circuit (circuit connection of 42 including the connection means) including a resistor and a capacitive device connected in series (see series connection of resistor formed by the connection means, and the capacitive device 42), and to a power supply 16 and the control inputs of the first and second transistors, the resistor being connected to the power supply and the capacitive device being connected to the control inputs of the first and second transistors.

3. Claims 1-3, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by John et al. (US 6,522,511). Regarding Claim 1, John discloses an integrated protection circuit for an integrated circuit device (Figures 1-3), comprising: a first transistor (PMOS of 32 in Figure 3) whose control outputs are connected between a pad 22 and a control input of a clamping device 34, control outputs of said clamping device being connected between said pad and a reference voltage terminal 20, a second transistor (NMOS of 32) whose control input of the clamping device and said reference voltage terminal, and time-delay means (resistor of 30 and the connection means) connected to a supply voltage terminal 18 and said control inputs of said first transistor and said second transistor.

Regarding Claim 2, John discloses that the pad 22 is a signal pad or a power supply pad. Regarding Claim 3, Jon discloses that the time- delay element comprises a series connection of a resistor and a capacitance (resistor element of 30 and the line capacitance of the connection means of R of 30 in Figure 3).

Regarding Claim 11, John discloses a diode 44 between the pad and the supply voltage terminal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US 5,617,283). Regarding Claim 5, Krakauer discloses that a fourth transistor 46 provided whose control outputs are connected between the reference voltage terminal and the control output of the third transistor. Krakauer does not disclose that that control input is connected to said reference voltage terminal (Krakauer has a diode connected MOS transistor whereas the claim recites a grounded gate MOS transistor). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a grounded gate MOS transistor, in place of a diode connected MOS transistor, because both connections remain off during normal operation of IC, and are used to clamp voltages during an ESD event, and differs only where the gate is connected to operate as a clamp, and the selection is based on the design requirements.

Regarding Claim 7, Krakauer discloses that the second and fourth transistors are n-channel MOS transistors. Krakauer does not disclose that the third transistor is n-channel MOS transistor (Krakauer's third transistor is a p-channel MOS transistor). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an n-channel MOS transistor for the third transistor also, because n-channel and p-channel MOS transistors are art recognized equivalents.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US 5,617,283) in view of Ker et al. (US 2002/0050615). Regarding Claim 10, Krakauer does not disclose a thyristor device. Ker discloses an ESD protection circuit (see Figure 7b) comprising a clamping device which is a thyristor (see

nSCR device). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the protection circuit of Krakauer, and to use a thyristor in place of the MOS transistor, because Ker teaches the use of thyristor as ESD clamping device for the protection of integrated circuits from ESD and EOS.

6. Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US 5,617,283) in view of Lai et al. (US 2003/0235022). Regarding Claims 11and 15, Krakauer does not disclose a diode between the pad and the supply voltage terminal. Lai discloses an ESD protection circuit comprising a diode 52 connected between a pad 40 and a power supply voltage terminal 50 (see Figure 4A). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the protection circuit of Krakauer, and to provide a diode as taught by Lai to provide and ESD path from PAD to the power supply pad to protect the IC and to isolate the pads during normal operation.

7. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over John et al. (US 6,522,511) in view of Avery t al. (US 6,501,632). Regarding Claim 12, John discloses an integrated protection circuit for protecting an integrated circuit device (Figures 1-3), the protection circuit comprising: a clamping device 34 having a control input and two control outputs , the control outputs including a first control output coupled to a pad 22 and a second control output coupled to a reference voltage terminal 20; a first transistor (PMOS transistor of inverter 32) having control outputs connected between the pad and the control input of the clamping device; a second transistor (NMOS transistor of 32) having control outputs connected between the reference

voltage terminal and the control input of the clamping device; and a time-delay circuit including a resistor and a capacitance connected in series (resistor element of 30 and the line capacitance of the connection means of R of 30 in Figure 3) and to a power supply 18 and the control inputs of the first and second transistors, the resistor being connected to the power supply and the capacitance being connected to the control inputs of the first and second transistors.

John differs as the line capacitance is used not that of a capacitive device. Avery discloses a time delay means RZ1, C (see Figure 3, resistor Rz1 is the parasitic resistance of device Z, and device Z is the capacitive device) connected between a pad 301 and control input of an NMOS transistor to control the on/off of the transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit of John, and to have the delay means as taught by Avery, to provide the delay dependent on the changes on one of the power supply to provide charging voltage to control the gate of the transistor as Avery teaches that a device with inherent/parasitic resistance and capacitance can be used as delay means.

Regarding Claim 13-15, John discloses that the capacitance is not directly coupled to the pad, the resistor is directly connected to the capacitive device with no intervening circuits, and a diode 44 coupled directly between the power supply and the output terminal with no intervening circuits, the diode adapted to mitigate current flow from the power supply to the output terminal (44 is reverse biased from 18 to 22).

Response to Arguments

8. Applicant's arguments filed on 10/07/2008 have been fully considered.

9. Regarding Applicant's arguments toward Krakauer and Jon references: Please see the new grounds of rejection. Regarding Claims 1, both Krakauer and Jon discloses all elements including a delay means connected between a supply voltage terminal and control inputs of the first and second transistor (Krakauer: circuit connection of 42 including the connection means, Jon: (resistor of 30 in Figure 3 and the connection means of the resistor).

Regarding Claim 12, Krakauer discloses all elements including a time-delay circuit including a resistor and a capacitive device connected in series (circuit connection of 42 including the connection means meets the limitation of time delay circuit with series connection of resistor formed by the connection means, and the capacitive device 42), and to a power supply 16 and the control inputs of the first and second transistors, the resistor being connected to the power supply and the capacitive device being connected to the control inputs of the first and second transistors.

Regarding Applicant's arguments toward Avery reference in Jon, Avery combination: Avery reference is relied upon for the teaching of a time delay circuit with a resistor and capacitive device in series, i.e., Avery teaches a device acting as a time delay means by providing a resistor and capacitance and that the device can be replaced with a capacitor, and keeping the resistor to have a resistor and capacitor in series. In Figure 3, Avery shows Rz1 and Z1, and teaches that Z1 can be replaced by a

capacitance, to result in Rz1 and C in series. Also note that Avery teaches a Zener Z4 and that it can be replaced by a resistor R.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yu et al. (US 4,802,054), Tyler et al. (US 2003/0202300).

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucy Thomas whose telephone number is 571-272-6002. The examiner can normally be reached on Monday - Friday 8:00 AM - 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. T./
Examiner, Art Unit 2836
January 06, 2009

/Stephen W Jackson/
Primary Examiner, Art Unit 2836